IN THE CLAIMS:

Please amend claims 1, 3, 5, 6, 8-10, 12-14, 16-19, 23, and 24 as follows:

1. (Currently Amended) An arithmetic circuit for use with ~~an RNS~~ a Residue Number System (RNS), said arithmetic circuit comprising:

an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs;

test circuitry coupled to the arithmetic core, the test circuitry ~~inducing~~ selectively feeding the output of the arithmetic core back to at least one of the inputs so as to induce oscillation at the output of the arithmetic core during testing; and

logic circuitry coupled to the output of the arithmetic core, the logic circuitry measuring an oscillation frequency of the output of the arithmetic core during testing and producing a pass/fail signal to indicate whether or not the input-to-output delay of the arithmetic core is within specification based on a determination of whether the oscillation frequency ~~of the arithmetic core~~ is at least equal to a minimum threshold value.

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2. (Original) The arithmetic circuit as defined in claim 1, wherein the logic circuitry includes:

a counter coupled to the output of the arithmetic core, the counter counting oscillations of the output during testing; and

a comparator coupled to the counter, the comparator comparing the output of the counter after a predetermined test period with the minimum threshold value and producing the pass/fail signal.

3. (Currently Amended) The arithmetic circuit as defined in claim 2, wherein the test circuitry includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and

at least one transmission gate for selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core ~~during testing~~.

4. (Original) The arithmetic circuit as defined in claim 3, wherein the isolation buffers, the transmission gate, and the counter are controlled by a test enable signal.

5. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the test circuitry includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and

at least one transmission gate for selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core ~~during testing~~.

6. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the test circuitry includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing;

a first transmission gate for selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core ~~during testing~~; and

a second transmission gate for selectively supplying a constant to the other input of the arithmetic core ~~during testing~~.

7. (Original) The arithmetic circuit as defined in claim 6, wherein the isolation buffers and the transmission gates are controlled by a test enable signal.

8. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the arithmetic core is ~~an OHRNS~~ a One-Hot Residue Number System (OHRNS) modulo m adder.

9. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the arithmetic core is ~~an OHRNS~~ a One-Hot Residue Number System (OHRNS) modulo m multiplier.

10. (Currently Amended) A digital signal processing device having at least one ~~RNS~~ Residue Number System (RNS) arithmetic circuit, said arithmetic circuit comprising:

an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs;

test circuitry coupled to the arithmetic core, the test circuitry ~~inducing~~ selectively feeding the output of the arithmetic core back to at least one of the inputs so as to induce oscillation at the output of the arithmetic core during testing; and

logic circuitry coupled to the output of the arithmetic core, the logic circuitry measuring an oscillation frequency of the output of the arithmetic core during testing and producing a pass/fail signal to indicate whether or not the input-to-output delay of the arithmetic core is within specification based on a determination of whether the oscillation frequency ~~of the arithmetic core~~ is at least equal to a minimum threshold value.

11. (Original) The digital signal processing device as defined in claim 10, wherein the logic circuitry of the arithmetic circuit includes:

a counter coupled to the output of the arithmetic core, the counter counting oscillations of the output during testing; and

a comparator coupled to the counter, the comparator comparing the output of the counter after a predetermined test period with the minimum threshold value and producing the pass/fail signal.

12. (Currently Amended) The digital signal processing device as defined in claim 11, wherein the test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and

at least one transmission gate for selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core ~~during testing~~.

13. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and

at least one transmission gate for selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core ~~during testing~~.

14. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing;

a first transmission gate for selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core ~~during testing~~; and

a second transmission gate for selectively supplying a constant to the other input of the arithmetic core ~~during testing~~.

15. (Original) The digital signal processing device as defined in claim 14, wherein the isolation buffers and the transmission gates are controlled by a test enable signal.

16. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the arithmetic core of the arithmetic circuit is ~~an OHRNS~~ a One-Hot Residue Number System (OHRNS) modulo m adder.

17. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the arithmetic core of the arithmetic circuit is ~~an OHRNS~~ a One-Hot Residue Number System (OHRNS) modulo m multiplier.

18. (Currently Amended) A method for testing propagation delay of ~~an RNS~~ a Residue Number System (RNS) arithmetic circuit incorporated into an integrated circuit device, the arithmetic circuit including an arithmetic core that performs an RNS arithmetic operation, said method comprising the steps of:

selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core[[;]] and selectively providing a constant to another input of the arithmetic core, so as to induce oscillation at the output of the arithmetic core during testing;

measuring an oscillation frequency of the output of the arithmetic core during testing; and

producing a pass/fail signal to indicate whether or not the propagation delay of the arithmetic core is within specification based on a determination of whether the oscillation frequency ~~of the arithmetic core~~ is at least equal to a minimum threshold value.

19. (Currently Amended) The method as defined in claim 18,

wherein the measuring step ~~of producing a pass/fail signal~~ includes the ~~sub-steps~~ sub-step of[[:]] counting oscillations of the output of the arithmetic core during a predetermined time period[[;]], and

the producing step includes the sub-step of comparing the counted oscillations with the minimum threshold value to determine a pass or fail condition.

20. (Original) The method as defined in claim 19, further comprising the step of isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing.

21. (Original) The method as defined in claim 18, further comprising the step of isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing.

22. (Original) The method as defined in claim 21, further comprising the step of supplying a test enable signal to start testing.

23. (Currently Amended) The method as defined in claim 18, wherein the arithmetic core is ~~an OHRNS~~ a One-Hot Residue Number System (OHRNS) modulo m adder.

24. (Currently Amended) The method as defined in claim 18, wherein the arithmetic core of the arithmetic circuit is ~~an OHRNS~~ a One-Hot Residue Number System (OHRNS) modulo m multiplier.